CLAIMS

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:

forming a lower metal interconnection over a substrate covered with an insulation layer;

providing an ILD including a lower barrier layer and an upper barrier layer that have an etch selectivity with respect to each other on the lower metal interconnection;

forming an etch mask for a via contact and anisotropically etching the ILD together with the upper barrier layer to expose the lower barrier layer;

isotropically etching the exposed lower barrier layer to form a via contact hole which has an undercut under the upper barrier layer and exposes a portion of the lower metal interconnection;

forming a barrier metal layer on an entire surface of the substrate where the via contact hole is formed, a portion of the barrier metal layer being discontinuously formed at the lower barrier layer; and

providing a metal layer on the barrier metal layer to fill the via contact hole.

2. The method as claimed in claim 1, wherein the lower metal interconnection and the metal layer are formed to have a copper layer.

3. The method as claimed in claim 1, wherein the lower metal interconnection is formed using a damascene method including:

forming a groove in the insulation layer;

stacking a thin barrier metal on the insulation layer having the groove;

stacking a metal layer on the barrier metal; and

performing CMP to expose a top surface of the insulation layer.

4. The method as claimed in claim 1, wherein the barrier metal layer is formed by sputtering.

5. The method as claimed in claim 1, wherein stacking the metal layer to fill the via contact hole comprises:

forming a metal seed layer on the barrier metal layer by a CVD method; and

forming the metal layer on the seed layer by an electroplating technique.

6. The method as claimed in claim 1, further comprising forming a groove in an upper portion of the ILD by a patterning process before or after forming the via contact hole,

wherein the via contact hole is formed at least directly under the groove, and wherein while the barrier metal layer and the metal layer are stacked to fill the via contact hole, the groove is also filled.

7. The method as claimed in claim 6, further comprising removing the metal layer and the barrier metal layer which are provided on the ILD by CMP, to expose a top surface of the ILD and to remain the metal layer in the via contact hole and the groove.

8. The method as claimed in claim 6, wherein the ILD is formed by sequentially stacking a first insulation layer, an etch stop layer, and a second insulation layer on the lower and upper barrier layers,

wherein forming the groove in the upper portion of the ILD when the groove is formed comprises patterning the second insulation layer or both the second insulation layer and the etch stop layer.